REMARKS

The foregoing amendments are responsive to the August 12, 2009 Office Action. Applicants respectfully request reconsideration of the present application in view of the foregoing amendments and the following remarks.

Response to Rejection of Claims 3-4, 7-8 and 23-26 Under 35 U.S.C. 102(b)

The Examiner rejected Claims 3-4, 7-8 and 23-26 under 35 U.S.C. 102(b) as being anticipated by Davies et al. (U.S. Patent No. 6,329,846).

Applicants respectfully argue that the Examiner has misconstrued the role of shunt transistors 410 and 411 of Figure 5 of Davies (US 6,329,846). Specifically, the shunt transistors 410, 411 do not help, and are not active, during pre-charge. The shunt transistor 410 and 411 are not provided to propagate a pre-charge wave, rather, the shunt transistors 410 and 411 are provided to make nodes AB and -AB immune to noise.

The nodes 405, 406 shown in Figure 5 of Davies are pre-charged by clock transistors 401. The nodes AB and -AB are pre-discharged by the NMOS transistors of invertors 403 and 404. This puts pre-discharged '0's on nodes AB and -AB. This means that the shunt transistors 410 and 411 are off during pre-discharge of nodes AB and -AB and they do not contribute.

To understand the actual function of transistors 410, 411, assume that at evaluation AB=1 and -AB=0. AB=1 is considered strong because there is a path to GND from node 405 through the NMOS transistors A, B and CLK of circuit 402. Because node 405 is a strong input to invertor 403, also node AB=1 is strong through the PMOS transistor of invertor 403 (where "strong" means there is a connection to VDD or GND). By contrast, -AB=0 is weak because node 406 is a 'floating' 1 during evaluation. This means that also -AB is possibly weak. However, shunt transistor 411 will connect -AB to a strong GND because its gate is connected to the strong AB. A similar argument can be made for AB=0 and -AB=1.

Moreover, this means that when cascading multiple circuits as shown in Davies, the pre-discharge operation will not be propagated from one such circuit to the next such circuit. Contrary to the arguments from the Examiner, the CLK signal is a crucial part of the full circuit depicted in Fig. 5 of Davies. The CLK signal is required to pre-discharge the output nodes AB

and -AB. Thus, as explained above, the circuit of Davies cannot propagate a pre-discharge wave as claimed.

Regarding Claim 3, the cited prior art does not teach or render obvious a wave dynamic differential logic, comprising a differential logic cell having inverted inputs and corresponding non-inverted inputs, the differential logic cell configured to provide one or more inverted logic outputs and corresponding one or more non-inverted logic outputs, the differential logic cell configured to propagate a pre-discharge wave.

Regarding Claim 4, the cited prior art does not teach or render obvious a differential logic cell having inverted inputs and corresponding non-inverted inputs, the differential logic cell configured to provide one or more inverted logic outputs and corresponding one or more non-inverted logic outputs, and a pre-discharged logic cell configured to generate a pre-discharge wave to pre-discharge the differential logic cell.

Regarding Claim 7, the cited prior art does not teach or render obvious a wave dynamic differential logic wherein a differential logic cell transmits a precharge value generated by a precharge generator.

Claims 23-26 depend, directly or indirectly, from Claim 3 and recite additional patentable limitations over and above those of Claim 3.

Accordingly, Applicants assert that Claims 3-4, 7-8 and 23-26 are allowable over prior art, and Applicants request allowance of Claims 3-4, 7-8 and 23-26.

Response to Rejection of Claims 5-6 and 9-12 Under 35 U.S.C. 103(a)

The Examiner rejected Claims 5-6 and 9-12 under 35 U.S.C. 103(a) as being unpatentable over Davies et al. in view of Forbes (U.S. Patent No. 6,437,604) and design choice case law. Davies is discussed above. Forbes merely discloses the complementary case.

Regarding Claim 5, the cited combination does not teach or render obvious a differential logic cell having inverted inputs and corresponding non-inverted inputs, the differential logic cell configured to provide one or more inverted logic outputs and corresponding one or more non-inverted logic outputs, and a master-slave differential dynamic logic register configured to generate a pre-charge wave to pre-charge the differential logic cell.

Regarding Claim 6, the cited combination does not teach or render obvious a differential logic cell having inverted inputs and corresponding non-inverted inputs, the differential logic cell configured to provide one or more inverted logic outputs and corresponding one or more non-inverted logic outputs, and a master-slave differential dynamic logic register configured to generate a pre-discharge wave to pre-discharge the differential logic cell.

Regarding Claim 9, the cited combination does not teach or render obvious a differential logic cell having inverted inputs and corresponding non-inverted inputs, the differential logic cell configured to provide one or more inverted logic outputs and corresponding one or more non-inverted logic outputs, and a master-slave differential dynamic logic register configured to transmit on a pre-charge wave to pre-charge the differential logic cell.

Regarding Claim 10, the cited combination does not teach or render obvious a differential logic cell having inverted inputs and corresponding non-inverted inputs, the differential logic cell configured to provide one or more inverted logic outputs and corresponding one or more non-inverted logic outputs, and a differential dynamic logic register configured to generate a pre-charge wave to pre-charge the differential logic cell.

Regarding Claim 11, the cited combination does not teach or render obvious a differential logic cell having inverted inputs and corresponding non-inverted inputs, the differential logic cell configured to provide one or more inverted logic outputs and corresponding one or more non-inverted logic outputs, and a master-slave differential dynamic logic register configured to transmit on a pre-discharge wave to pre-discharge the differential logic cell.

Regarding Claim 12, the cited combination does not teach or render obvious a differential logic cell having inverted inputs and corresponding non-inverted inputs, the differential logic cell configured to provide one or more inverted logic outputs and corresponding one or more non-inverted logic outputs, and a differential dynamic logic register configured to generate a pre-discharge wave to pre-discharge the differential logic cell.

Accordingly, Applicants assert that Claims 5-6 and 9-12 are allowable over prior art, and Applicants request allowance of Claims 5-6 and 9-12.

No Disclaimers or Disavowals

Although the present communication may include alterations to the application or claims, or characterizations of claim scope or referenced art, Applicant is not conceding in this application that previously pending claims are not patentable over the cited references. Rather, any alterations or characterizations are being made to facilitate expeditious prosecution of this application. Applicant reserves the right to pursue at a later date any previously pending or other broader or narrower claims that capture any subject matter supported by the present disclosure, including subject matter found to be specifically disclaimed herein or by any prior prosecution. Accordingly, reviewers of this or any parent, child or related prosecution history shall not reasonably infer that Applicant has made any disclaimers or disavowals of any subject matter supported by the present application.

Co-Pending Applications of Assignee

Applicant wishes to draw the Examiner's attention to the following co-pending applications of the present application's assignee.

Docket No.	Serial No.	Title	Filed
UCLARF.002NP	10/554,763	System for Biometric Signal Processing With Hardware and Software Acceleration	August 7, 2006
UCLARF.003DV1	12/191,144	Dynamic and Differential CMOS Logic With Signal-Independent Power Consumption to Withstand Differential Power Analysis	August 13, 2008
UCLARF.003NP	10/565,551	Dynamic and Differential CMOS Logic With Signal-Independent Power Consumption to Withstand Differential Power Analysis	September 11, 2006
UCLARF.008NP	12/092,687	Methods and Apparatus for Context-Sensitive Telemedicine	October 29, 2008
UCLARF.010A	12/167,062	Signal Decoder With General Purpose Calculation Engine	July 2, 2008

Summary

Applicants respectfully assert that Claims 1-26 are in condition for allowance, and Applicants request allowance of Claims 1-26. If there are any remaining issues that can be resolved by a telephone conference, the Examiner is invited to call the undersigned attorney at (9449) 721-6305 or at the number listed below.

Please charge any additional fees, including any fees for additional extension of time, or credit overpayment to Deposit Account No. 11-1410.

Respectfully submitted,

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Dated: November 12, 2009

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